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Claims

[c1] 1. A memory structure comprising:
a transistor having an emitter, a base, and a collector, said base having a lower surface adjacent an insulating layer; and
a base contact comprising a phase change material.

[c2] 2. The memory structure of Claim 1, wherein said transistor induces phase changes in said phase change material.

[c3] 3. The memory structure of Claim 1, wherein said phase change material comprises a chalcogenide alloy.

[c4] 4. The memory structure of Claim 3, wherein said chalcogenide alloy comprises $Ge_2Sb_2Te_5$.

[c5] 5. The memory structure of Claim 1, wherein at least a portion of said phase change material is positioned on an upper surface of said base.

[c6] 6. The memory structure of Claim 1, wherein said emitter is n-type, said base is p-type, said collector is n-type and said base contact is p-type polysilicon.

[c7] 7. The memory structure of Claim 1, wherein said emitter is p-type, said base is n-type, said collector is p-type and said base contact is n-type polysilicon.

[c8] 8. The memory structure of Claim 1, wherein said insulating layer comprises a buried oxide (BOX) layer of a silicon-on-insulator substrate.

[c9] 9. A semiconductor structure comprising:
a substrate comprising a first doped region flanked by a set of second doped regions;
a phase change material positioned on said first doped region; and
a conductor positioned on said phase change material, wherein when said phase change material comprises a first phase said semiconductor structure operates as a bipolar junction transistor, and when said phase change material comprises a second phase said semiconductor structure operates as a field effect transistor.

[c10] 10. The semiconductor structure of Claim 9, wherein said phase change material comprises a chalcogenide alloy.

[c11] 11. The semiconductor structure of Claim 10, wherein said chalcogenide alloy comprises $Ge_2Sb_2Te_5$.

[c12] 12. The semiconductor structure of Claim 9,wherein said

first phase comprises a crystalline solid phase.

[c13] 13. The semiconductor structure of Claim 9, wherein said second phase comprises an amorphous solid phase.

[c14] 14. The semiconductor structure of Claim 9, wherein said phase change material is converted to said first phase or said second phase by heat radiating from said substrate.

[c15] 15. A method of forming a memory device comprising:
providing an initial structure comprising a sacrificial gate atop a first conductivity region in a Si-containing layer of an SOI substrate, said sacrificial gate flanked by a set of spacers;
forming second conductivity regions abutting said first conductivity region in said Si-containing layer;
removing said sacrificial gate to provide a gate via;
forming a phase change material liner within at least a portion of said gate via; and
forming a gate conductor on said phase change material liner.

[c16] 16. The method of Claim 15, wherein said phase change material liner comprises a chalcogenide alloy.

[c17] 17. The method of Claim 15, wherein said phase change material liner has a thickness of less than about 20 nm.

[c18] 18. The method of Claim 15 wherein said sacrificial gate comprises polysilicon.

[c19] 19. The method of Claim 18 wherein said removing said sacrificial gate comprises etching said sacrificial gate with KOH.

[c20] 20. The method of Claim 15 wherein forming said phase change material liner comprises sputtering or chemical vapor deposition (CVD) at temperatures less than about 600°C.